CLAIMS

1. A transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

a p-type region disposed over said n-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a control gate disposed above and insulated from said channel;

said substrate, said n-type region and said p-type region each biased such that said p-type region is fully depleted.

2. The transistor of claim 1 wherein said n-type region is a well region.

3. The transistor of claim 1 wherein said p-type region is a well region.

4. The transistor of claim 2 wherein said n-type region is a well region.

5. The transistor of claim 1 wherein said n-type region is a buried layer.

6. The transistor of claim 5 wherein said n-type region is a buried layer laid out in a grid formation.

7. The transistor of claim 1 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said n-type region.

8. A transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

n-type buried layers disposed at about a boundary between said substrate and said n-type region, said buried layers doped to a higher level than said n-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a control gate disposed above and insulated from said channel; and

said substrate, said n-type region and said n-type buried layers each biased such that said n-type region is fully depleted.

9. The transistor of claim 8 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.

10. A floating-gate transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

a p-type region disposed over said n-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a floating gate disposed above and insulated from said channel; and

said substrate, said n-type region and said p-type region each biased such that said p-type region is fully depleted.

11. The floating-gate transistor of claim 10 wherein said n-type region is a well region.

12. The floating-gate transistor of claim 10 wherein said p-type region is a well region.

13. The floating-gate transistor of claim 11 wherein said n-type region is a well region.

14. The floating-gate transistor of claim 10 wherein said n-type region is a buried layer.

15. The floating-gate transistor of claim 14 wherein said n-type region is a buried layer laid out in a grid formation.

16. The floating gate transistor of claim 10 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said n-type region;

17. A floating-gate transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

n-type buried layers disposed at about a boundary between said substrate and said n-type region, said buried layers doped to a higher level than said n-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a floating gate disposed above and insulated from said channel;

a control gate disposed above and insulated from said floating gate; and

said substrate, said n-type region and said n-type buried layers each biased such that said n-type region is fully depleted.

18. The floating-gate transistor of claim 16 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.

19. A transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

an n-type region disposed over said p-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a control gate disposed above and insulated from said channel; and

said substrate, said p-type region and said n-type region each biased such that said n-type region is fully depleted.

20. The transistor of claim 19 wherein said p-type region is a well region.

21. The transistor of claim 19 wherein said n-type region is a well region.

22. The transistor of claim 20 wherein said p-type region is a well region.

23. The transistor of claim 19 wherein said p-type region is a buried layer.

24. The transistor of claim 23 wherein said p-type region is a buried layer laid out in a grid formation.

25. The transistor of claim 19 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said p-type region.

26. A transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

p-type buried layers disposed at about a boundary between said substrate and said p-type region, said buried layers doped to a higher level than said p-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a control gate disposed above and insulated from said channel; and

said substrate, said p-type region and said p-type buried layers each biased such that said p-type region is fully depleted.

27. The transistor of claim 26 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.

28. A floating-gate transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

an n-type region disposed over said p-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a floating gate disposed above and insulated from said channel; and

said substrate, said p-type region and said n-type region each biased such that said n-type region is fully depleted.

29. The floating-gate transistor of claim 28 wherein said p-type region is a well region.

30. The floating-gate transistor of claim 28 wherein said n-type region is a well region.

31. The floating-gate transistor of claim 29 wherein said p-type region is a well region.

32. The floating-gate transistor of claim 28 wherein said p-type region is a buried layer.

33. The floating-gate transistor of claim 32 wherein said p-type region is a buried layer laid out in a grid formation.

34. The floating gate transistor of claim 28 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said p-type region.

35. A floating-gate transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

p-type buried layers disposed at about a boundary between said substrate and said p-type region, said buried layers doped to a higher level than said p-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a floating gate disposed above and insulated from said channel;

a control gate disposed above and insulated from said floating gate;

and

said substrate, said p-type region and said p-type buried layers each biased such that said p-type region is fully depleted.

36. The floating-gate transistor of claim 35 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.